CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A magnetic random access memory cell comprising:

a first magnetic storage element having a first sense layer and a first pinned layer;

a second magnetic storage element having a second sense layer and a second pinned layer, said first and second sense layers being mutually electrically coupled through first and second read conductors, said first and second read conductors having respective longitudinal axes, said first and second pinned layers being electrically coupled to respective first and second read/write conductors, said first and second read/write conductors having at least localized longitudinal axes in respective vicinities of said first and second magnetic storage elements, said at least localized longitudinal axes of said first read/write conductor being oriented substantially parallel to said longitudinal axis of said first read conductor;

a switching device having a first controlled terminal coupled to said mutually coupled pinned layers through said first and second read conductors, a second controlled terminal coupled to a source of substantially constant potential, and a control terminal adapted to receive a control signal.

2. A magnetic random access memory cell as defined in claim 1 wherein said source of substantially constant potential comprises a source of ground potential.

3. A magnetic random access memory cell as defined in claim 1 wherein said first magnetic storage element and said second magnetic storage element are disposed above said switching device in a first direction, and wherein said switching device is disposed beside a further switching device of a further magnetic random access memory cell in a second direction.

4. A memory device comprising:

a plurality of read/write conductor pairs;

at least one memory cell electrically coupled between each of said read/write conductor pairs, said at least one memory cell including a controllable transistor and exactly two resistive memory elements, said exactly two resistive memory elements being coupled in series, said exactly two resistive memory elements being mutually coupled to said controllable transistor at a common node.

5. A memory device as defined in claim 4 wherein:

said exactly two resistive memory elements each include a pinned layer and a sense layer; and

wherein said sense layer of each said resistive memory element is electrically coupled through said controllable transistor to a source of substantially constant electrical potential.

6. A memory device as in claim 5 wherein said source of substantially constant electrical potential is a source of ground potential.

7. A memory device as defined in claim 4 wherein said controllable transistor comprises: two transistors having a common drain connection and respective gate terminals, said gate terminals mutually coupled to one another.

8. A memory device as defined in claim 4 wherein:

said first and second resistive memory elements are disposed in layered spaced relation to one another above said controllable transistor.

9. A memory device as defined in claim 4 further comprising:

a word line conductor electrically coupled to a gate of said controllable transistor.

10. A memory integrated circuit comprising:

a first two-dimensional array of resistive memory elements disposed in substantially parallel spaced relation between a second two-dimensional array of resistive memory elements and a third two-dimensional array of isolation devices, each isolation device of said third two-dimensional array being coupled to at least one resistive memory element of said first two-dimensional array and at least another resistive memory element of said second two-dimensional array;

a first plurality of read/write conductors having respective longitudinal axes oriented in a first direction and coupled to said first two-dimensional array of resistive memory elements; and

a second plurality of read conductors having respective longitudinal axes also oriented in said first direction and also coupled to said first two-dimensional array of resistive memory elements.

11. A memory integrated circuit as defined in claim 10 wherein said first array of resistive memory elements comprises an array of MRAM memory elements.

12. A memory integrated circuit as defined in claim 10 wherein said first array of resistive memory elements comprises an array of PCRAM memory elements.

13. A memory integrated circuit as defined in claim 10 further comprising:

a sensing circuit, said sensing circuit adapted to sense a state of said resistive memory elements during a time interval when a respective isolation device is activated.

14. A memory integrated circuit comprising:

a plurality of memory cells, each cell including:

first and second resistive memory storage elements, said first and second resistive memory storage elements being electrically coupled to respective first and second memory sensing circuits, said first and second resistive memory storage elements being mutually coupled to a reference potential through a common dual transistor.

15. A memory integrated circuit as defined in claim 14 wherein said first and second resistive memory storage elements are disposed in spaced relation above said common dual transistor.

16. A memory integrated circuit as defined in claim 14 further comprising an address decoder electrically coupled to first and second gates of said dual transistor and adapted to activate said dual transistor in response to an address signal received at an address input of said address decoder.

17. A magnetic random access memory device comprising:

a semiconductor substrate having an upper surface;

a controlled transistor having a drain region disposed on said semiconductor substrate;

a first magnetic random access memory storage element disposed above said upper surface and above said drain region in spaced relation thereto and electrically coupled to said drain region through a first read conductor, said first read conductor having a first longitudinal axis;

a second magnetic random access memory storage element disposed above said upper surface and above said first magnetic random access memory storage element in spaced relation thereto and electrically coupled to said first magnetic random access memory storage element and electrically coupled to said drain region through a second read conductor, said second read conductor having a second longitudinal axis; and

first and second read/write conductors having respective third and fourth longitudinal axes, said first longitudinal axis being disposed substantially parallel to said third longitudinal axis, said second longitudinal axis being disposed substantially parallel to said fourth longitudinal axis.

18. A PCRAM device comprising:

a semiconductor substrate having an upper surface;

a controlled transistor having a drain region disposed on said semiconductor substrate;

a first PCRAM storage element disposed above said upper surface and above said drain region in spaced relation thereto and electrically coupled to said drain region through a first read conductor, said first read conductor having a first longitudinal axis;

a second PCRAM storage element disposed above said upper surface and above said first PCRAM storage element in spaced relation thereto and electrically coupled to said first PCRAM storage element and electrically coupled to said drain region through a second read conductor, said second read conductor having a second longitudinal axis; and

first and second read/write conductors having respective third and fourth longitudinal axes, said first longitudinal axis being disposed substantially parallel to said third longitudinal axis, said second longitudinal axis being disposed substantially parallel to said fourth longitudinal axis.

19. A method of manufacturing a digital data storage device comprising:

forming a transistor layer, including a first plurality of controlled transistors, over a semiconductor substrate;

forming a first resistive memory storage layer over said transistor layer, said first resistive memory storage layer including a second plurality of resistive memory storage structures, said first resistive memory storage layer including a third plurality of read conductors and a fourth plurality of read/write conductors, said third plurality of read conductors and said fourth plurality of read/write conductors having a fifth plurality of longitudinal axes and sixth plurality of longitudinal axes respectively, said fifth plurality of longitudinal axes being disposed in substantially parallel relationship to said sixth plurality of longitudinal axes;

forming a second magnetic memory storage layer, including a seventh plurality of magnetic memory storage structures, over said first magnetic memory storage layer; and

electrically coupling respective ones of said first plurality of controlled transistors, said second plurality of magnetic memory storage structures, and said seventh plurality of magnetic memory storage structures to form a respective plurality of multi-bit transistor isolated magnetic memory cells.

20. A method of manufacturing a digital data storage device as defined in claim 19 further comprising:

forming a control circuit over said semiconductor substrate, said control circuit being adapted to activate said first plurality of controlled transistors.

21. A processing system comprising:

a plurality of memory cells, each cell including:

first and second resistive memory storage elements, said first and second resistive memory storage elements being electrically coupled to respective first and second memory sensing circuits, said first and second resistive memory storage elements being mutually coupled to a reference potential through a wired-NOR FLASH memory style transistor.

22. A method of forming a memory device comprising:

forming a first plurality of FLASH-memory style transistors disposed in a first array above a semiconductor substrate;

forming a second plurality of resistive memory elements disposed in a second array above said first array;

forming a third plurality of resistive memory elements disposed in a third array above said second array; and

electrically coupling a resistive memory element of said third plurality to a respective resistive memory element of said second plurality and to a respective FLASH-memory style transistor of said first plurality.